CLAIMS

What is claimed is:

1. An apparatus comprising:

a storage area to hold a first source data having a plurality of data elements;

a functional unit to perform operations specified by a packed data instruction set having a format identifying the first source data and a second source data, wherein said packed data instruction set specifies operations including one or more packed shift type operations, said funtional unit including

a shifter circuit to shift the first source data in response to the one or more packed shift type operations; and

a correction circuit to generate a corresponding replacement digit for each data element of the plurality of data elements, the correction circuit coupled to the shifting circuit to produce a result packed data comprising, as separate result elements, said first source data having each data element shifted by an amount specified by said second source data with said amount of bits for each data element filled, if needed, with the corresponding replacement digit.

2. The apparatus of Claim 1 wherein said one or more packed shift type operations include:

one or more packed shift right arithmetic type operations that each cause said result packed data to comprise, as separate result elements, said first source data having each data element shifted to the right said amount specified by said second source data with high order bits filled, if needed, with a sign value;

one or more packed shift left type operations that each cause said result packed data to comprise, as separate result elements, said first source data having each data element shifted to the left said amount specified by said second source data with low

order bits filled, if needed, with a zero; and

one or more packed shift right logical type operations that each cause said result packed data to comprise, as separate result elements, said first source data having each data element shifted to the right said amount specified by said second source data with high order bits filled, if needed, with a zero.

3. The apparatus of Claim 1 wherein the packed data instruction set has a format permitting a first three-bit source-destination address and a second three-bit source address identifying the first source data and the second source data respectively.

4. The apparatus of Claim 3 wherein bits three through five of said format correspond to the first three-bit source-destination address and bits zero through two of said format correspond to the second three-bit source address.

5. The apparatus of Claim 1 wherein the packed data instruction set has a format permitting a first byte to include a first three-bit source-destination address identifying the first source data and a second three-bit opcode extension identifying the second source data as an immediate value following said first byte.

6. The apparatus of Claim 5 wherein bits zero through two of said first byte correspond to the first three-bit source-destination address and bits three through five of said first byte correspond to the second three-bit opcode extension.

7. The apparatus of Claim 1 wherein the packed data instruction set has a format permitting register by memory addressing to identify the first source data and the second source data respectively.

8. The apparatus of Claim 1 wherein the packed data instruction set has a format permitting an operation code to specify one or more packed shift operations to perform

an arithmetic right shift of word elements or of doubleword elements from the first packed data.

9. The apparatus of Claim 8 wherein the one or more packed shift operations to perform the arithmetic right shift causes each result data element to be filled with a corresponding sign value when the second source data represents a value greater than fifteen for packed word elements or a value greater than thirty-one for packed doubleword elements.

10. The apparatus of Claim 1 wherein the packed data instruction set has a format permitting an operation code to specify one or more packed shift operations to perform a logical right shift of word elements or of doubleword elements from the first packed data.

11. The apparatus of Claim 10 wherein the one or more packed shift operations to perform the logical right shift causes each result data element to be filled with a zero value when the second source data represents a value greater than fifteen for packed word elements or greater than thirty-one for packed doubleword elements

12. A method comprising:

accessing a first source data having a plurality of data elements from a first storage area;

accessing a second source data from a second storage area; and

enabling a functional unit to perform a packed shift operation specified by a packed data instruction having a format identifying the first source data and the second source data, wherein performing said packed shift operation includes

shifting the first packed data in response to the packed shift operation, and

generating a replacement value for each data element of the plurality of

data elements, to produce a result packed data comprising, as separate result elements, said first source data having each data element shifted by an amount specified by said second source data with said amount of bits for each data element filled, if needed, with the corresponding replacement value.

13. The method of Claim 12 wherein said packed shift operation is one of a set of packed shift right arithmetic type operations that each cause said result packed data to comprise, as separate result elements, said first source data having each data element shifted to the right said amount specified by said second source data with high order bits filled, if needed, with a sign value.

14. The method of Claim 12 wherein said packed shift operation is one of a set of one or more packed shift left type operations that each cause said result packed data to comprise, as separate result elements, said first source data having each data element shifted to the left said amount specified by said second source data with low order bits filled, if needed, with a zero.

15. The method of Claim 12 wherein said packed shift operation is one of a set of one or more packed shift right logical type operations that each cause said result packed data to comprise, as separate result elements, said first source data having each data element shifted to the right said amount specified by said second source data with high order bits filled, if needed, with a zero. .

16. The method of Claim 12 wherein performing said packed shift operation further includes replacing all bits of each data element of said first source data with the corresponding replacement value if the amount specified by said second source data is greater than the number of bits in each data element.

17. The method of Claim 12 wherein the packed data instruction has a format including a first three-bit source-destination address and a second three-bit source address identifying the first source data and the second source data respectively.

18. The method of Claim 17 wherein bits three through five of said format correspond to the first three-bit source-destination address and bits zero through two of said format correspond to the second three-bit source address.

19. The method of Claim 12 wherein the packed data instruction format has a first byte to include a first three-bit source-destination address identifying the first source data and a second three-bit opcode extension identifying the second source data as an immediate value following said first byte.

20. The method of Claim 19 wherein bits zero through two of said first byte correspond to the first three-bit source-destination address and bits three through five of said first byte correspond to the second three-bit opcode extension.

21. The method of Claim 12 wherein the packed data instruction has a format permitting register by memory addressing to identify the first source data and the second source data respectively.

22. The method of Claim 12 wherein the packed data instruction specifies the packed shift operation to perform an arithmetic right shift on word elements or doubleword elements from the first packed data.

23. The method of Claim 12 wherein the packed data instruction specifies the packed shift operation to perform a logical right shift of word elements or of doubleword elements from the first packed data.

24. An article of manufacture comprising

a machine-accessible medium including data that, when accessed by a machine, causes the machine to perform the method of Claim 12.

25. An article of manufacture comprising

a machine-accessible medium including design data suitable to at least one process technology, said design data to implement an apparatus to perform the method of Claim 12.

26. A system comprising:

a memory to hold a plurality of data elements;

a processor to perform operations specified by a packed data instruction set having a format identifying a first source data and a second source data, wherein said packed data instruction set specifies operations including one or more packed shift type operations, said processor including:

a storage area to store the plurality of data elements as the first source data;

a shifter circuit to shift the first source data in response to the one or more packed shift type operations, and

a correction circuit to generate a corresponding replacement digit for each data element of the plurality of data elements, the correction circuit coupled to the shifting circuit to produce a result packed data comprising, as separate result elements, said first source data having each data element shifted by an amount specified by said second source data with said amount of bits for each data element filled, if needed, with the corresponding replacement digit;

a bus coupled with the processor to transmit data to and from the processor and to and from the memory; and

an interface to couple the bus with one or more devices to provide data to or receive data from the bus, said one or more devices comprising an audio device selected from the group consisting of an audio digitizing device, a sound recording device, a sound playback device, a microphone, a digital-to-analog converter, and a speaker.

27. The system of Claim 26 wherein said one or more packed shift type operations include:

one or more packed shift right arithmetic type operations that each cause said result packed data to comprise, as separate result elements, said first source data having each data element shifted to the right said amount specified by said second source data with high order bits filled, if needed, with a sign value;

one or more packed shift left type operations that each cause said result packed data to comprise, as separate result elements, said first source data having each data element shifted to the left said amount specified by said second source data with low order bits filled, if needed, with a zero; and

one or more packed shift right logical type operations that each cause said result packed data to comprise, as separate result elements, said first source data having each data element shifted to the right said amount specified by said second source data with high order bits filled, if needed, with a zero.

28. The system of Claim 26 further comprising

a storage device to store a plurality of instruction sequences including instructions of the packed data instruction set, said storage device to couple with the bus to transmit instructions to the processor and to the memory, wherein the plurality of instruction sequences include at least an instruction sequence to manipulate audio.

29. The system of Claim 26 further comprising

a storage device to store a plurality of instruction sequences including

instructions of the packed data instruction set, said storage device to couple with the bus to transmit instructions to the processor and to the memory, wherein the plurality of instruction sequences include at least an instruction sequence to perform voice recognition.